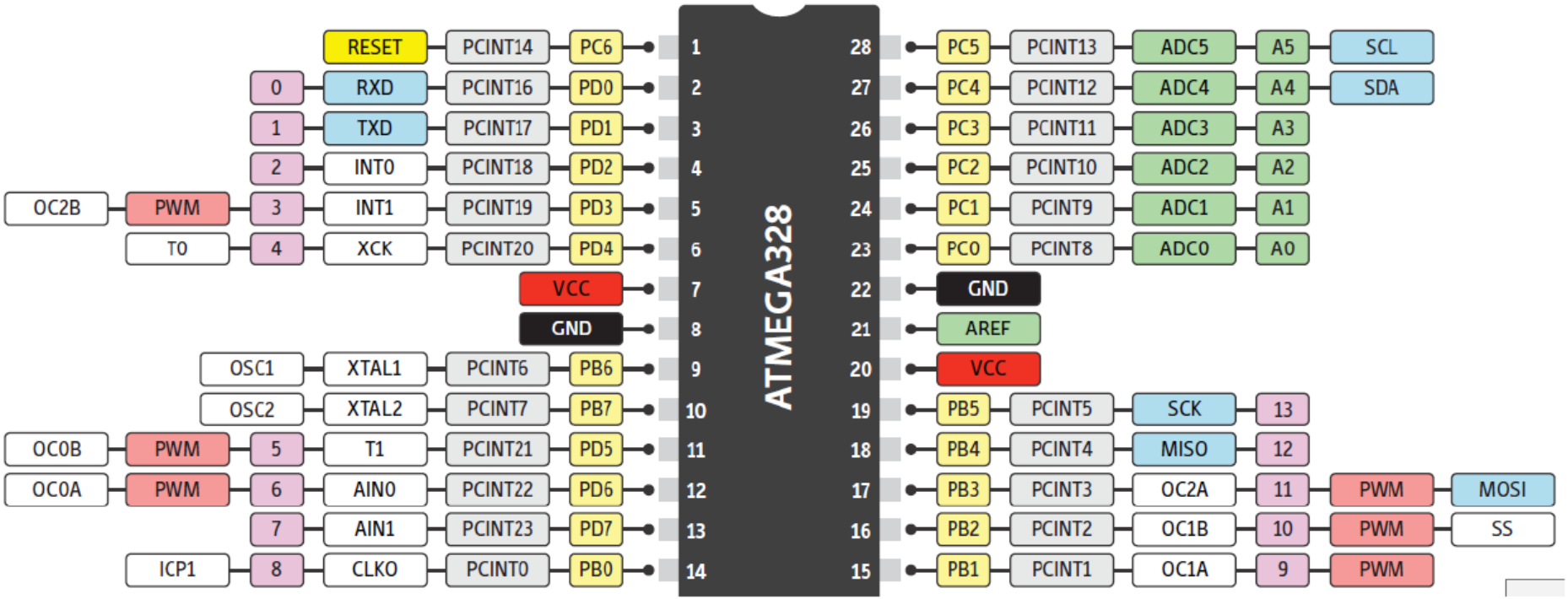
PRIMENA MIKROKONTROLERA

Analogno-digitalni konvertor ADC

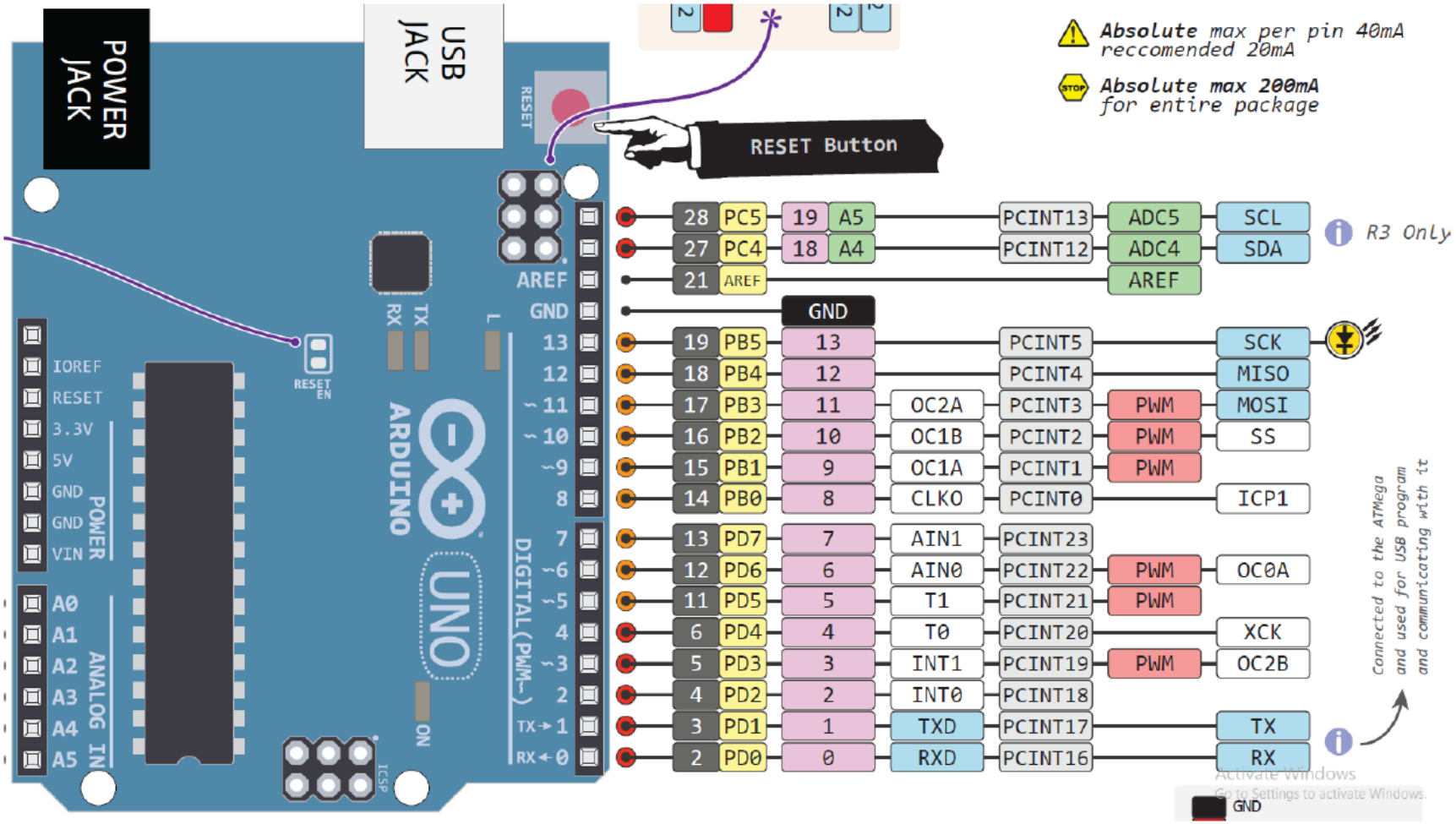
prof. dr Zoran Milivojević
dr Nataša Nešić, viši predavač

Mikrokontroler ATmega328P



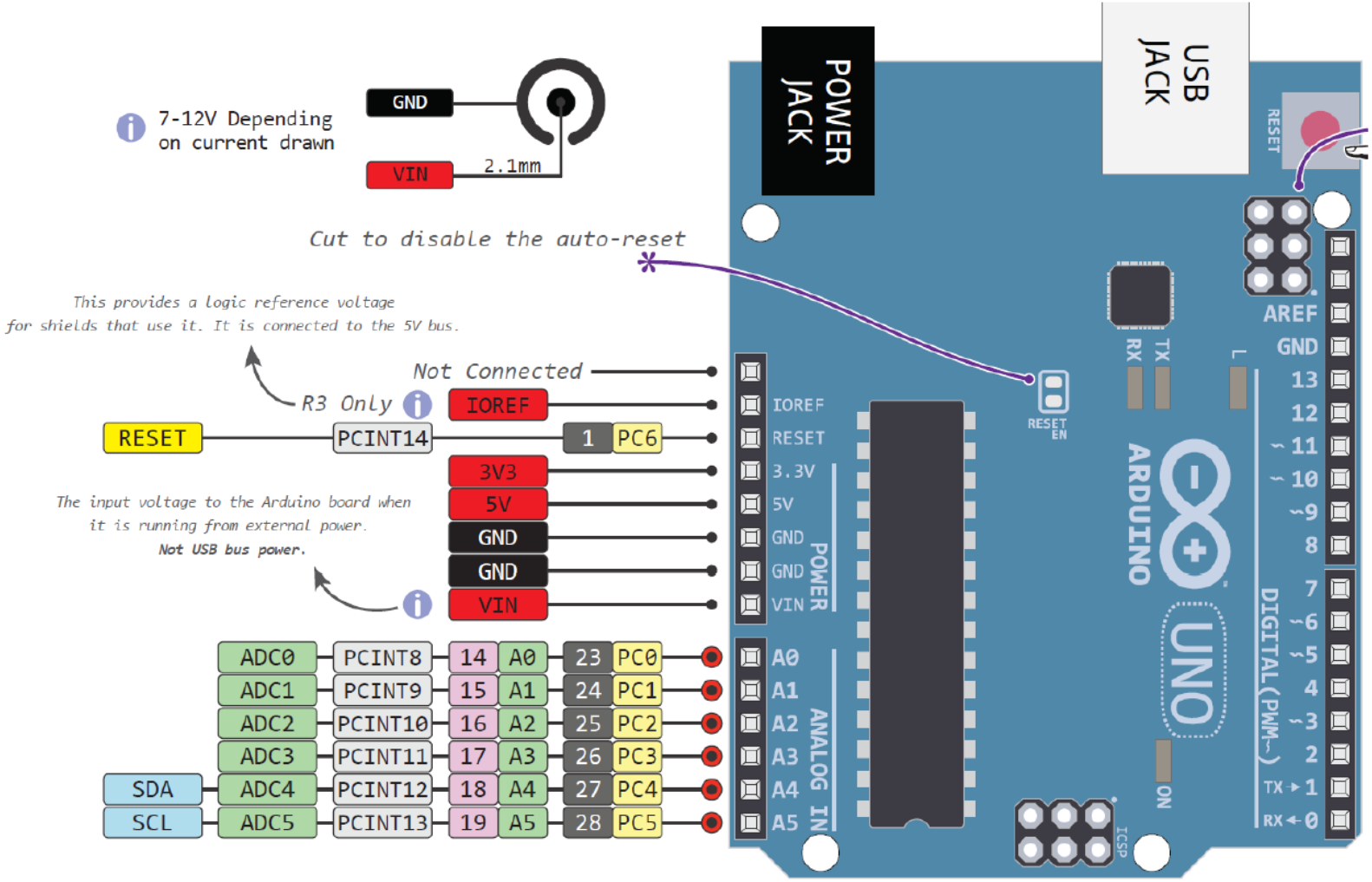
Slika 1. *PINOUT dijagram mikrokontrolera ATmega328P.*

Arduino UNO

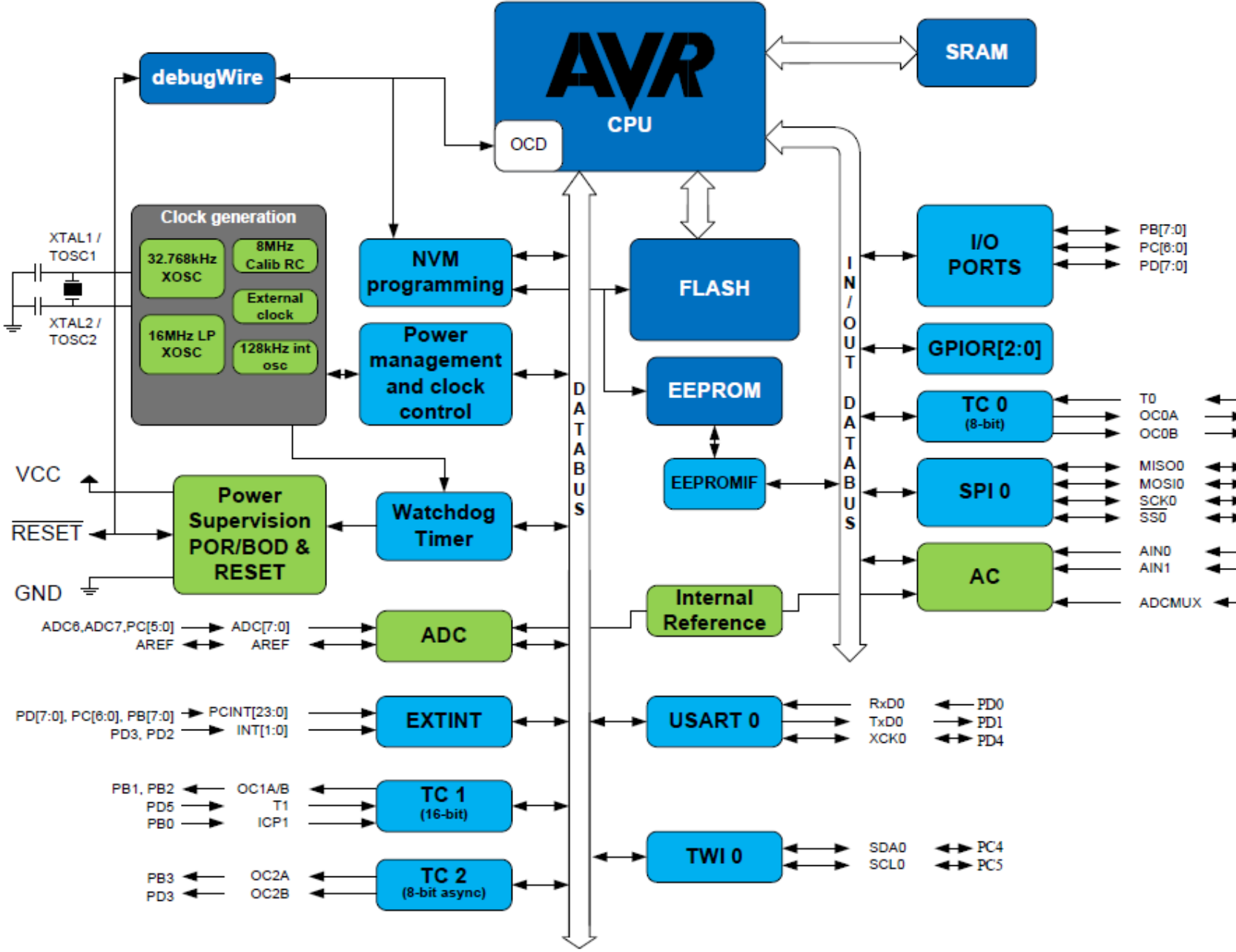


Slika 5. *Deo 2 pinout dijagram Arduino UNO sistema.*

Arduino UNO



Slika 4. *Deo 1 pinout dijagram Arduino UNO sistema.*

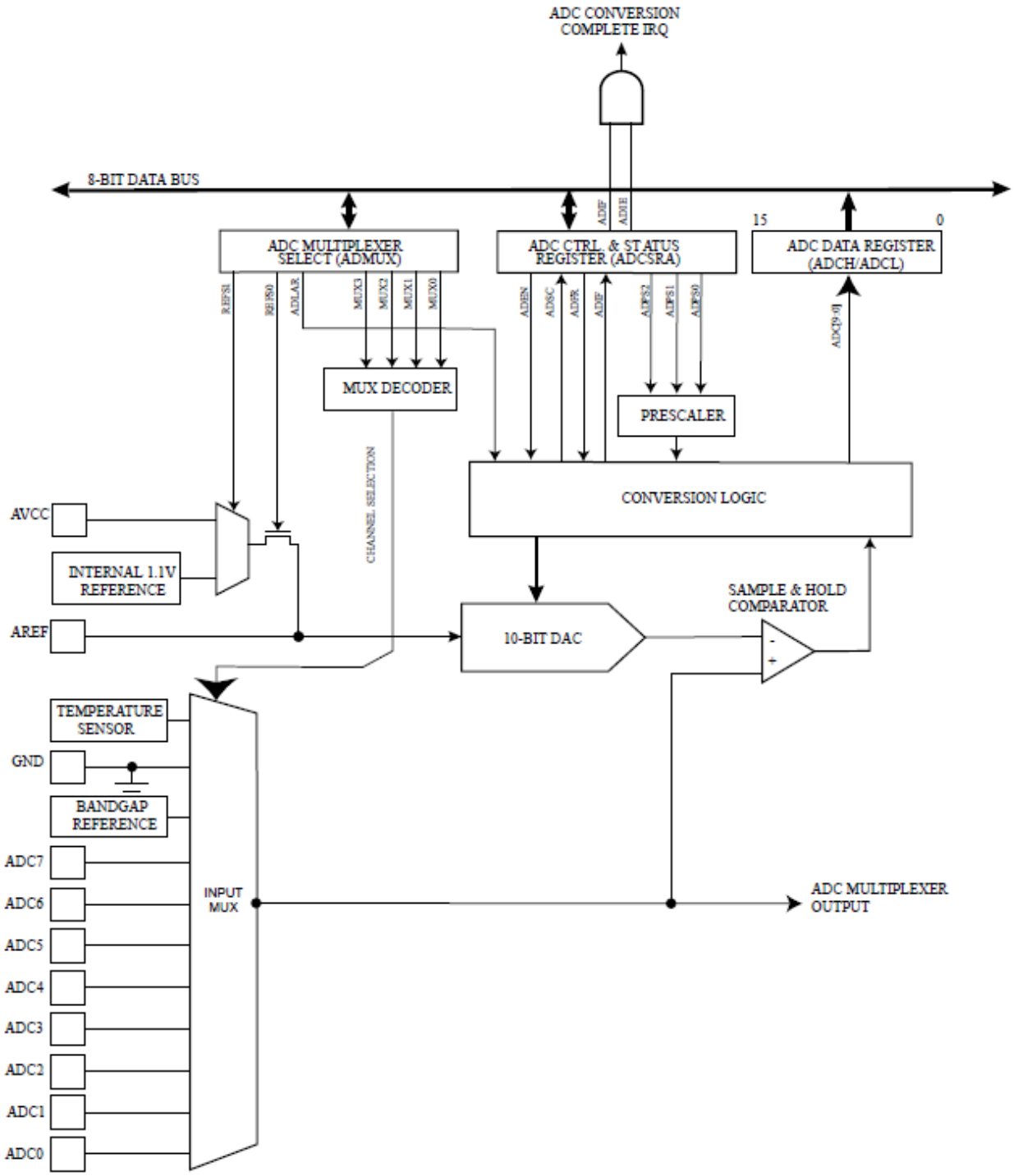

AVR
CPU
OCD
debugWire
SRAM
Clock generation
32.768kHz XOSC
8MHz Calib RC
External clock
16MHz LP XOSC
128kHz int osc
XTAL1 / TOSC1
XTAL2 / TOSC2
NVM programming
Power management and clock control
FLASH
EEPROM
EEPROMIF
DATABUS
I/O DATABUS
I/O PORTS
PB[7:0]
PC[6:0]
PD[7:0]
GPIOR[2:0]
TC 0 (8-bit)
T0
OC0A
OC0B
SPI 0
MISO0
MOSI0
SCK0
SS0
AC
AIN0
AIN1
ADCMUX
VCC
RESET
GND
Power Supervision POR/BOD & RESET
Watchdog Timer
Internal Reference
ADC
ADC6,ADC7,PC[5:0]
AREF
ADC[7:0]
AREF
EXTINT
PD[7:0], PC[6:0], PB[7:0]
PD3, PD2
PCINT[23:0]
INT[1:0]
USART 0
RxD0
TxD0
XCK0
PD0
PD1
PD4
TC 1 (16-bit)
PB1, PB2
PD5
PB0
OC1A/B
T1
ICP1
TWI 0
SDA0
SCL0
PC4
PC5
TC 2 (8-bit async)
PB3
PD3
OC2A
OC2B

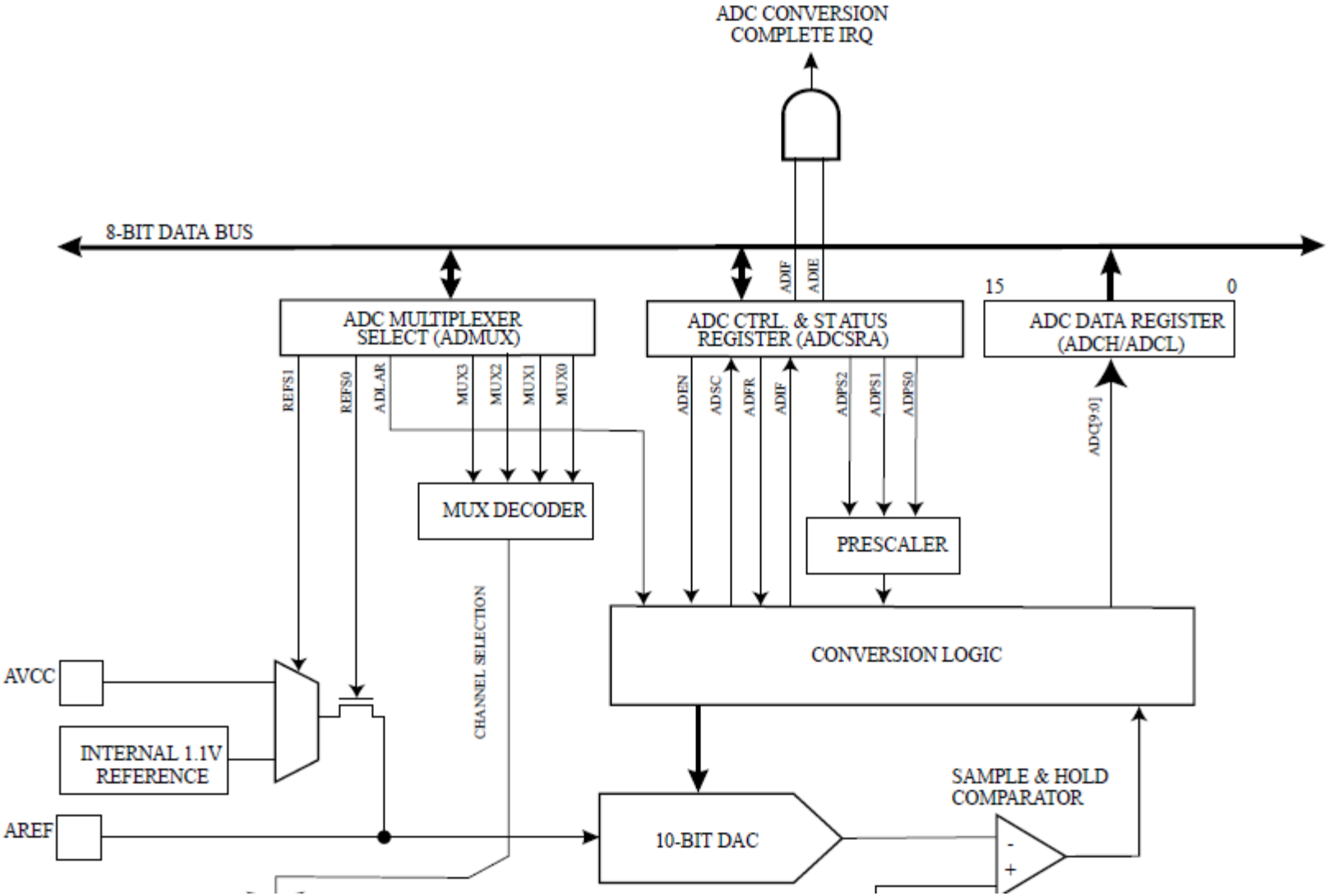
Karakteristike ADC

- Karakteristike integrisanog Analogno-digitalnog konvertora su:
  - 10-bitna rezolucija
  - 13-260 µs vreme konverzije
  - 6 ulaznih analognih multipleksiranih kanala
  - dva dodatna analogna kanala kod TQFP i VFQFN kućišta
  - Kanal temperaturnog senzora
  - Kanal naponskog referentnog izvora 1.1 V
  - Napon ulaznih kanala u opsegu 0-Vcc
  - Aktiviranje prekida

ADC

- Integrisani ADC je sa sukcesivnom aproksimacijom
- To znači da se u koracima približava tačnoj vrednosti
- Vreme završetka konverzije je različito za pojedine naponske nivoe
- Završetak konverzije može biti u opsegu 13-260 µs
- Završetak konverzije označava se flegom i generisanjem zahteva za prekidom.
- rezultat konverzije upisan je u ADCH i ADCL 8-bitne registre.
- U ADCL su 8 bita a u ADCH koriste se samo dva bita, tako da je rezultat konverzije 10-bit.


ADC CONVERSION COMPLETE IRQ
8-BIT DATA BUS
ADIF
ADIE
15
0
ADC MULTIPLEXER SELECT (ADMUX)
ADC CTRL. & STATUS REGISTER (ADCSRA)
ADC DATA REGISTER (ADCH/ADCL)
REFS1
REFS0
ADLAR
MUX3
MUX2
MUX1
MUX0
ADEN
ADSC
ADFR
ADIF
ADPS2
ADPS1
ADPS0
ADC[9:0]
MUX DECODER
PRESCALER
CHANNEL SELECTION
CONVERSION LOGIC
AVCC
INTERNAL 1.1V REFERENCE
AREF
10-BIT DAC
SAMPLE & HOLD COMPARATOR
TEMPERATURE SENSOR
GND
BANDGAP REFERENCE
ADC7
ADC6
ADC5
ADC4
ADC3
ADC2
ADC1
ADC0
INPUT MUX
ADC MULTIPLEXER OUTPUT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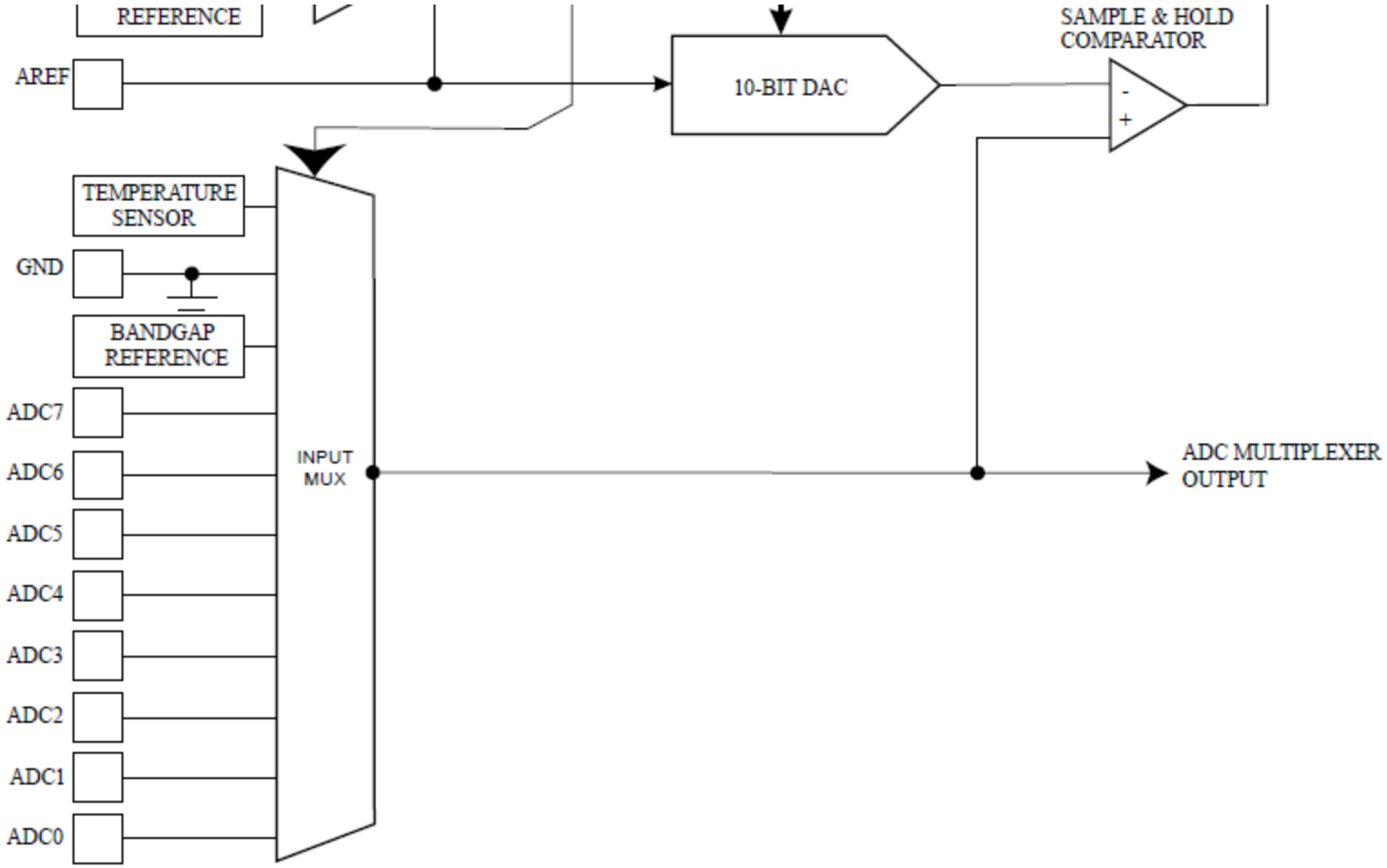
AREF
SAMPLE & HOLD COMPARATOR
10-BIT DAC
-
+

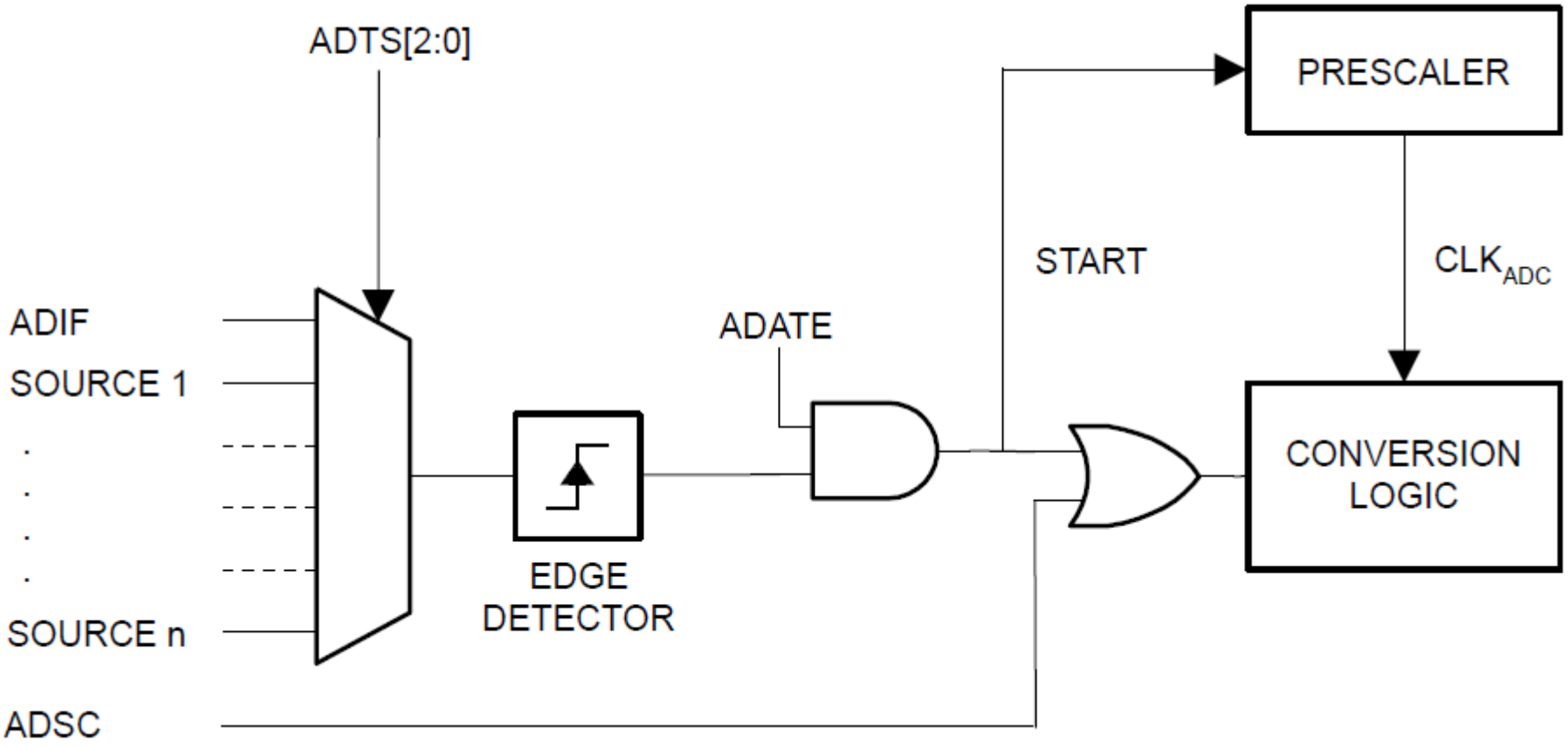
Ulazni signali za konverziju

- Signali za konverziju modu biti
- 8 ekstern2 (sa pinova mikrokontrolera)
- 2 interna (temperaturni senzor i referentni napon 1.1 V)
- Selektovanje signala za konverziju ostvaruje se pomoću ulaznog selektora MUX (vremensko multipleksiranje)
- Upravljanje radom multipleksera vrši se programom postavljanjem pojedinih bitova u ADMUX registru.

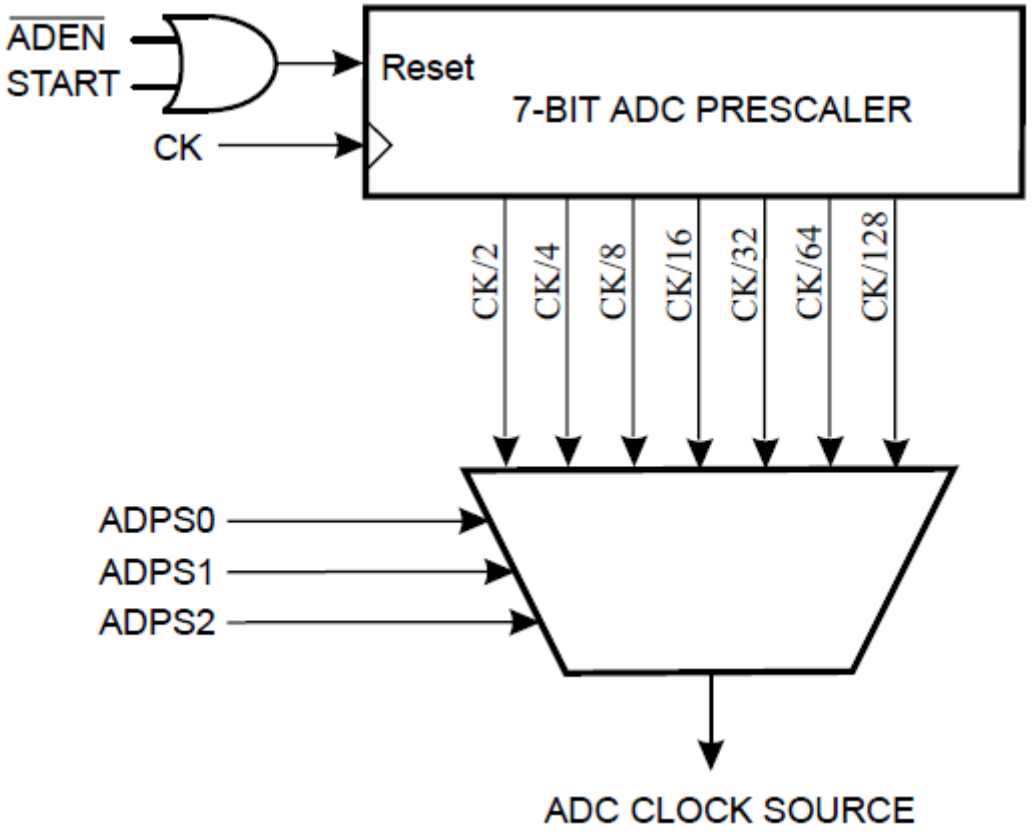

REFERENCE
AREF
10-BIT DAC
SAMPLE & HOLD
COMPARATOR
-
+
TEMPERATURE
SENSOR
GND
BANDGAP
REFERENCE
ADC7
ADC6
ADC5
ADC4
ADC3
ADC2
ADC1
ADC0
INPUT
MUX
ADC MULTIPLEXER
OUTPUT

ADC

- Dozvola rada ADC ostvaruje se upisom log. 1 u bit ADEN u registru ADCSRA (ADC Control and Status Register)
- Početak konverzije je upisom log. 1 u ADSC bit ADCSRA registra.
- Konverzija može da počne i trigerovanjem signalima iz
  - Brojača T/C0
  - Brojača T/C1
  - Analognog komparatora
  - flega zahteva za prekidom (Free Running Mode)


ADTS[2:0]
PRESCALER
START
CLK ADC
ADIF
SOURCE 1
ADATE
CONVERSION
LOGIC
EDGE
DETECTOR
SOURCE n
ADSC

Kontrola takta ADC



Free Running Mode

- Startovanje ADC pomoću ADC interrupt flega obezbeđuje se da konverzija krene kada je predhodna konverzija završena.
- Izvršenje prekida, pod uslovom da je prekid dozvoljen, ne narušava rad AD konvertora.

ADC Multiplexer Selection Register

Name: ADMUX
Offset: 0x7C
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	REFS1	REFS0	ADLAR		MUX3	MUX2	MUX1	MUX0
Access	R/W	R/W	R/W		R/W	R/W	R/W	R/W
Reset	0	0	0		0	0	0	0

Bits 7:6 – REFSn: Reference Selection [n = 1:0]
These bits select the voltage reference for the ADC. If these bits are changed during a conversion, the change will not go in effect until this conversion is complete (ADIF in ADCSRA is set). The internal voltage reference options may not be used if an external reference voltage is being applied to the AREF pin.

Table 28-3. ADC Voltage Reference Selection

REFS[1:0]	Voltage Reference Selection
00	AREF, Internal V_{ref} turned off
01	AV_{CC} with external capacitor at AREF pin
10	Reserved
11	Internal 1.1V Voltage Reference with external capacitor at AREF pin

ADC Multiplexer Selection Register

Bit 5 – ADLAR: ADC Left Adjust Result

The ADLAR bit affects the presentation of the ADC conversion result in the ADC Data Register. Write one to ADLAR to left adjust the result. Otherwise, the result is right adjusted. Changing the ADLAR bit will affect the ADC Data Register immediately, regardless of any ongoing conversions. For a complete description of this bit, see ADCL and ADCH.

Bits 3:0 – MUXn: Analog Channel Selection [n = 3:0]

The value of these bits selects which analog inputs are connected to the ADC. If these bits are changed during a conversion, the change will not go in effect until this conversion is complete (ADIF in ADCSRA is set).

Table 28-4. Input Channel Selection

MUX[3:0]	Single Ended Input
0000	ADC0
0001	ADC1
0010	ADC2
0011	ADC3
0100	ADC4
0101	ADC5

ADC Multiplexer Selection Register

MUX[3:0]	Single Ended Input
0110	ADC6
0111	ADC7
1000	Temperature sensor
1001	Reserved
1010	Reserved
1011	Reserved
1100	Reserved
1101	Reserved
1110	1.1V (V_{BG})
1111	0V (GND)

ADC Control and Status Register A

Name: ADCSRA
Offset: 0x7A
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – ADEN: ADC Enable
Writing this bit to one enables the ADC. By writing it to zero, the ADC is turned off. Turning the ADC off while a conversion is in progress, will terminate this conversion.

Bit 6 – ADSC: ADC Start Conversion
In Single Conversion mode, write this bit to one to start each conversion. In Free Running mode, write this bit to one to start the first conversion. The first conversion after ADSC has been written after the ADC has been enabled, or if ADSC is written at the same time as the ADC is enabled, will take 25 ADC clock cycles instead of the normal 13. This first conversion performs initialization of the ADC.

ADSC will read as one as long as a conversion is in progress. When the conversion is complete, it returns to zero. Writing zero to this bit has no effect.

ADC Control and Status Register A

Bit 5 – ADATE: ADC Auto Trigger Enable
When this bit is written to one, Auto Triggering of the ADC is enabled. The ADC will start a conversion on a positive edge of the selected trigger signal. The trigger source is selected by setting the ADC Trigger Select bits, ADTS in ADCSRB.

Bit 4 – ADIF: ADC Interrupt Flag
This bit is set when an ADC conversion completes and the Data Registers are updated. The ADC Conversion Complete Interrupt is executed if the ADIE bit and the I-bit in SREG are set. ADIF is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, ADIF is cleared by writing a logical one to the flag. Beware that if doing a Read-Modify-Write on ADCSRA, a pending interrupt can be disabled. This also applies if the SBI and CBI instructions are used.

Bit 3 – ADIE: ADC Interrupt Enable
When this bit is written to one and the I-bit in SREG is set, the ADC Conversion Complete Interrupt is activated.

Bits 2:0 – ADPSn: ADC Prescaler Select [n = 2:0]
These bits determine the division factor between the system clock frequency and the input clock to the ADC.

ADC Control and Status Register A

ADPS[2:0]	Division Factor
000	2
001	2
010	4
011	8
100	16
101	32
110	64
111	128

ADC Data Register Low

Name: ADCL
Offset: 0x78
Reset: 0x00
Property: ADLAR = 0

Bit	7	6	5	4	3	2	1	0
	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – ADCn: ADC Conversion Result [n = 7:0]
These bits represent the result from the conversion. Refer to ADC Conversion Result for details.

ADC Data Register High

Name: ADCH
Offset: 0x79
Reset: 0x00
Property: ADLAR = 0

Bit	7	6	5	4	3	2	1	0
							ADC9	ADC8
Access							R	R
Reset							0	0

Bit 1 – ADC9: ADC Conversion Result
Refer to ADCL.

Bit 0 – ADC8: ADC Conversion Result

ADC Control and Status Register B

Name: ADCSRB
Offset: 0x7B
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
		ACME				ADTS2	ADTS1	ADTS0
Access		R/W				R/W	R/W	R/W
Reset		0				0	0	0

Bit 6 – ACME: Analog Comparator Multiplexer Enable
When this bit is written logic one and the ADC is switched off (ADEN in ADCSRA is zero), the ADC multiplexer selects the negative input to the Analog Comparator. When this bit is written logic zero, AIN1 is applied to the negative input of the Analog Comparator. For a detailed description of this bit, see *Analog Comparator Multiplexed Input*..

ADC Control and Status Register B

Bits 2:0 – ADTSn: ADC Auto Trigger Source [n = 2:0]

If ADATE in ADCSRA is written to one, the value of these bits selects which source will trigger an ADC conversion. If ADATE is cleared, the ADTS[2:0] settings will have no effect. A conversion will be triggered by the rising edge of the selected Interrupt Flag. Note that switching from a trigger source that is cleared to a trigger source that is set, will generate a positive edge on the trigger signal. If ADEN in ADCSRA is set, this will start a conversion. Switching to Free Running mode (ADTS[2:0]=0) will not cause a trigger event, even if the ADC Interrupt Flag is set.

Table 28-6. ADC Auto Trigger Source Selection

ADTS[2:0]	Trigger Source
000	Free Running mode
001	Analog Comparator
010	External Interrupt Request 0
011	Timer/Counter0 Compare Match A
100	Timer/Counter0 Overflow
101	Timer/Counter1 Compare Match B
110	Timer/Counter1 Overflow
111	Timer/Counter1 Capture Event

- **HVALA NA PAŽNJI**